Spread Spectrum Transceiver for Wireless Local Area Networks

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ABSTRACT

The wireless communications have become very important in the last few years. One of the most important branches of wireless communications is the Wireless Local Area Networks (WLAN) that are used to transfer data, voice and image between mobile nodes in the ISM band. In this paper the specifications, design, simulation and implementation of a wireless local area network transceiver based on Direct Sequence Spread Spectrum (DSSS) technology is presented. This transceiver has a data rate of 9.6 kbps, a chip rate of 144 kcps with maximum length code and carrier frequency of 1152 kHz and makes full use of Binary Phase Shift Keying (BPSK).

KEYWORDS

Local Area Networks; Spread Spectrum; Direct sequence, Spread Spectrum Transceiver.

I.INTRODUCTION

The widespread uses of notebook computers and handheld personal digital assistants have led to an increased dependence on wireless LANs in recent years. At physical layer the IEEE 802.11 defines three physical layers for WLAN's classified according to the transmission technique that is used [1]: -

1- Infrared (IR) LANs 2- Spread spectrum LANs 3- Narrowband LANs

The most important and most commonly used type of Wireless LAN's is the Spread Spectrum LAN's that make use of spread spectrum transmission technology.

The definition of spread spectrum modulation is stated in the following two parts [2]: -

1- Spread spectrum (SS) is a means of transmission in which the data sequence occupies a bandwidth in excess of the minimum bandwidth necessary to send it.

2-The spectrum spreading is accomplished before transmission through the use of a code that is independent of the data sequence. The same code is used in the receiver (operating in synchronism with the transmitter) to despread the received signal so that the original data sequence may be recovered. The IEEE.802.11 standard specifies only two types of SS systems that are used in wireless LANs. These two types are namely Direct Sequence (DS) and Frequency Hopping (FH). DSSS works by taking a data stream of zeros and ones and modulating it with a second pattern called the chipping sequence which is an 11-bit (chip) sequence (10110111000) called Barker code [3]. The chipping or spreading code is used to generate a redundant bit pattern to be transmitted, and the resulting signal appears as wide band noise to the unintended receiver. In this work design, simulation and implementation of a Direct Sequence Spread Spectrum transceiver is introduced. This transceiver is used for Wireless Local Area Networks. The worked out specifications of the transceiver are data rate of 9.6 kbps, processing gain of 15, the code used is maximum length code, the distance range is 100 m, modulation type used is BPSK, carrier frequency is 1152 KHz and transmitted power is less than 1w.

II.BLOCK DIAGRAM FOR SIMULATION

The paper focuses attention to all signal processing blocks except the high frequency part. The simulation block diagram according to the Matlab building blocks is depicted in Fig (1). In this model the data source is entered to BPSK modulator block, and then the BPSK signal is spread by multiplication with the

Pseudo Noise (PN) code. In the receiving part the reverse process is done where the despreading process is achieved by multiplying the received signal with a synchronized PN replica and then demodulation process takes place. Typical waveforms at each test point of the transceiver are plotted in Fig (2-a). In this figure the data is used to bi-phase modulates the carrier. Then the resulting BPSK is directly multiplied by the PN code so the spreading process is accomplished.

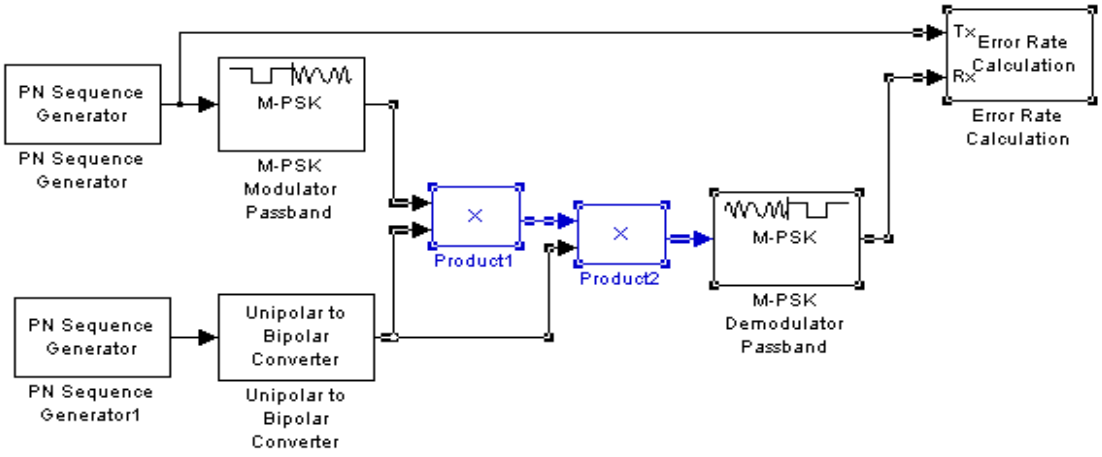


Fig (1) First DSSS model by Matlab

Fig (2-b) represents the simulation waveforms in the receiver, where a despreading process is done by multiplying the received DSSS signal with a synchronized PN code. Then a demodulation process takes place to retrieve the data. By comparing the input and the output data sequence in Fig (2-C) the output data waveform coincides with the input data waveform except some delay of the output data due to transmission processing and /or transmission time.

In the previous model we notice that the modulation process is performed before the spreading process this configuration is simpler in analysis but depends on the use of analog multiplier to multiply the modulated signal with the code. Another model which performs the spreading process before the modulation process is also introduced. This model uses an XNOR logical device as a digital multiplier which is very simpler than the analog multiplier. The simulation waveforms of the signal in the transmitter and receiver are shown in Fig (3).Basically; they are similar to those of the preceding model (because spreading process and modulating process are both linear [4]) except the occurrence of spikes at each transition of the chip pulses. Consequently the main problem with this model is in the receiver where the demodulated chips (digital) must be multiplied digitally by the PN code which must be delayed with the same amount of delay that the chips were undergone due to propagation. Even if the code generated is synchronized with the chips a very little phase shift still found as shown in Fig (3-b). So a Low Pass Filter (LPF) must be used to clean the data signal.

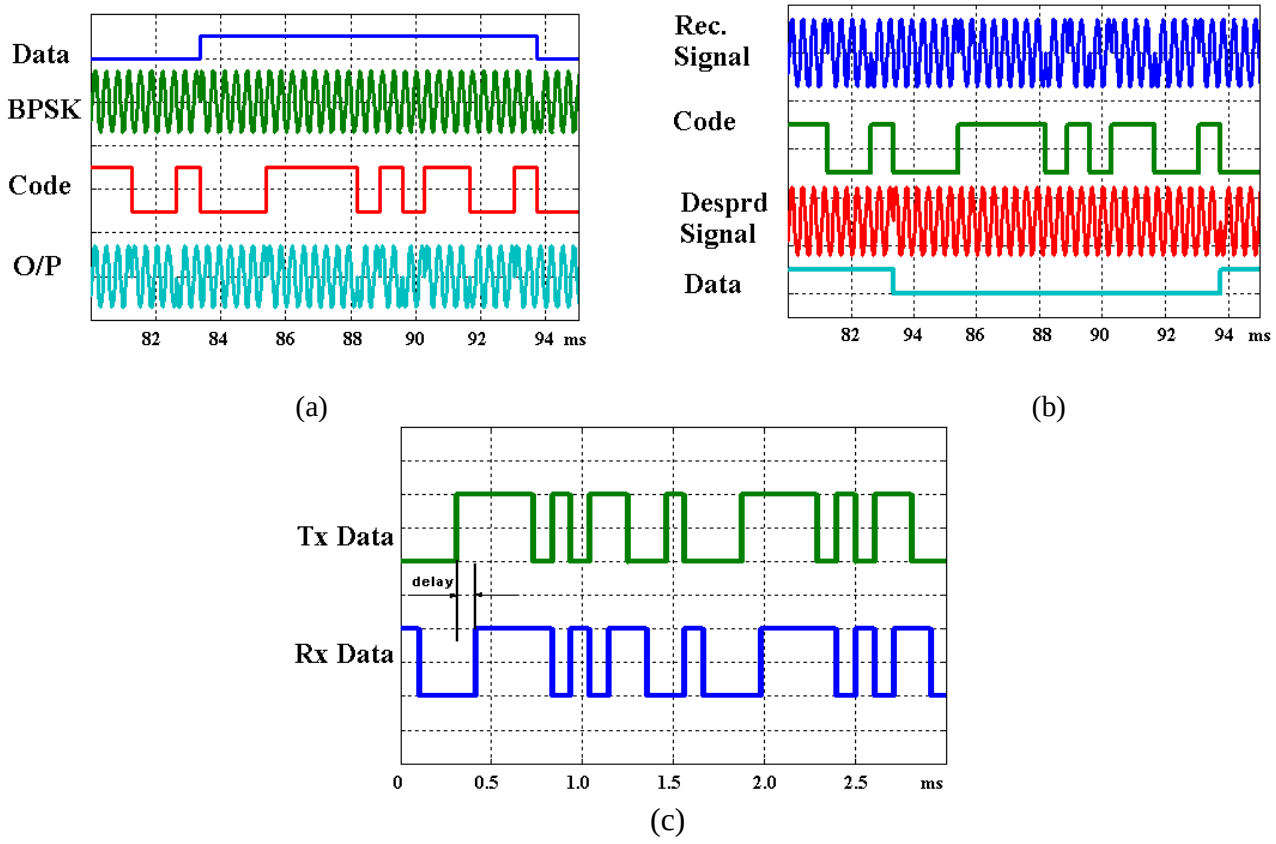


Fig (2) (a) Transmitter waveforms (b) Receiver Waveforms (c) Transmitted & Received Data

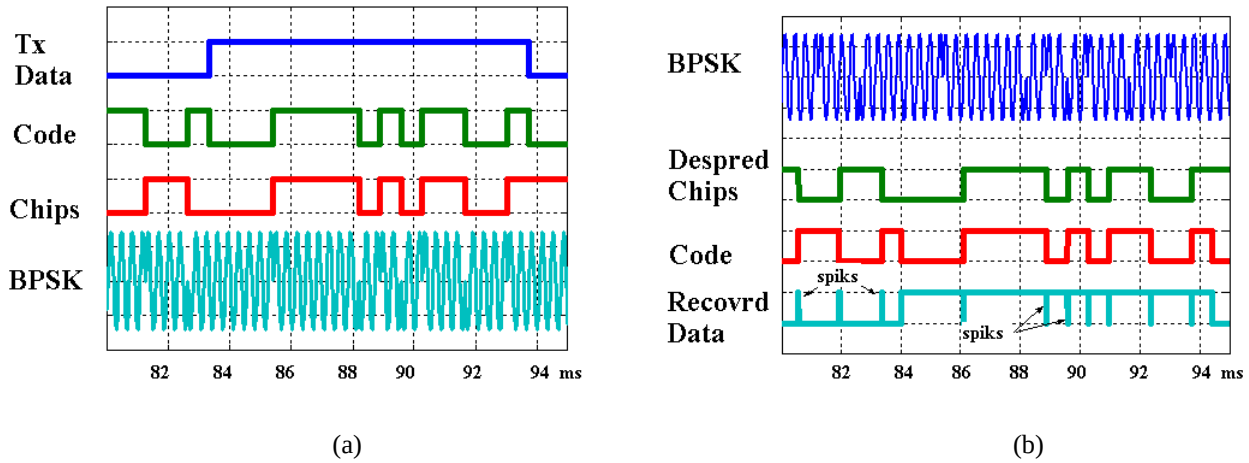


Fig (3) (a) Second model transmitter waveforms (b) Second model receiver waveforms

III.TRANSMITTER IMPLEMENTATION

To implement the transmitter it is easier to divide it into two parts. The first part is the timing circuit then the second part is the modulating circuit.

1-The Timing Circuit

This circuit is responsible for generating the auxiliary signals required in the transmitter circuit such as the clock pulses for PN code generator, clock pulses for data generator and the carrier required for BPSK modulator. It is very important in the transmitter that all above mentioned signals to begin at the same moment to achieve transmitter synchronization. One method to achieve that synchronization in transmitter is to make all signals to be emitted from the same source. The realized circuit diagram of the timing circuit is shown in Fig (4). A crystal oscillator of 16.128 MHz rectangular clock pulses is used as source of all timing circuit signals .Then a divide by14 counter (IC 74161) is used to divide the 16.128 MHz and generate 1152 KHz clock pulses. This output is then fed to another counter (IC4040) to divide it by 8; the output is at frequency of 144 KHz clock pulses which is used to generate the PN code. This output is fed to another 74161 counter loaded by 1 to make division by 15 and produces 9.6 KHz clock pulses used to generate the data from a hypothetical source at the transmitter. After the generation of the required clock pulses shown in Fig (6-a) we still need to generate the carrier and an 180^{o} degree phase shifted one synchronized with the data bits and the code. We used the 1152 KHz rectangular pulses to generate the carrier by selecting the fundamental frequency using a RLC series resonance circuit. The fundamental frequency is sinusoidal wave of 1152 KHz which is entered to a phase splitting circuit to have +SIN &- SIN shown in Fig (6-b).

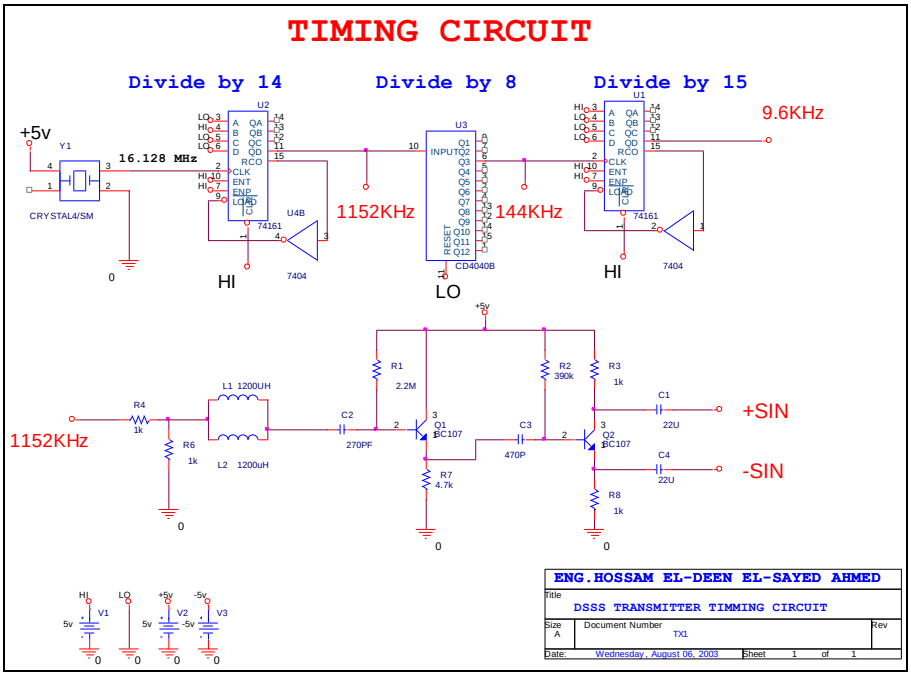


Fig (4) The implemented circuit diagram of Timing Circuit

2-Modulating Circuit

This circuit represents the rest of the transmitter. It contains two types of modulation; first the spreading process and second the BPSK modulation. This circuit is shown in Fig (5).

The spreading process requires digital multiplication of data stream with a PN code then BPSK modulation occurs. The circuit in Fig (5) is divided into four parts as follows:

1- Data source

Here we assume the data source to be either a computer or for simplicity we can assume a PN code at data rate (9.6 Kbps) to be a data source. This assumption enables us to see the input and output of spreading circuit more clearly on the oscilloscope.

2- PN code

The design of PN code essentially requires a shift register with an XOR logic feedback. The shift register is achieved by an IC 74164. This chip has a unique initial state of all zeros that is forbidden in the design of the maximum length codes when using XOR logic. So we use XNOR logic to insure that all zero state of the shift register will not continue and then we invert the final output of the PN code. This has the same effect of using a shift register with all ones initial state and XOR feed back logic. We use a [4, 1] maximum length sequence of length 15 [5] which has the waveform shown in Fig (6-c).

3- The Digital Multiplier

We use an XNOR as a digital multiplier which is simpler than the analog one. After the digital multiplier each bit in the data stream has chopped into 15 bit of PN code as shown by the oscillegram of Fig (6-d). It is clear from the figure that the code is inverted for data bit one and remains unchanged for data bit zero. This is simply the result of the multiplication process.

4- BPSK Modulator

The practical BPSK modulator used is simpler than the Balanced Modulator and analog multiplier. The +sin and –sin signals that have been generated by the timing circuit are used as inputs of an analog multiplexer. The CD4053 analog multiplexer selects between the two inputs (+sin and –sin) according to a select signal which is actually the digital chips that emerge from the spreading process in the digital multiplier. The output of 4053 is +sin when select input is zero and the output is –sin when it is logic one

The measured output of this stage is displayed in Fig (6-e). The phase shift keying is very apparent from the phase reversals at the edges of the code chips.

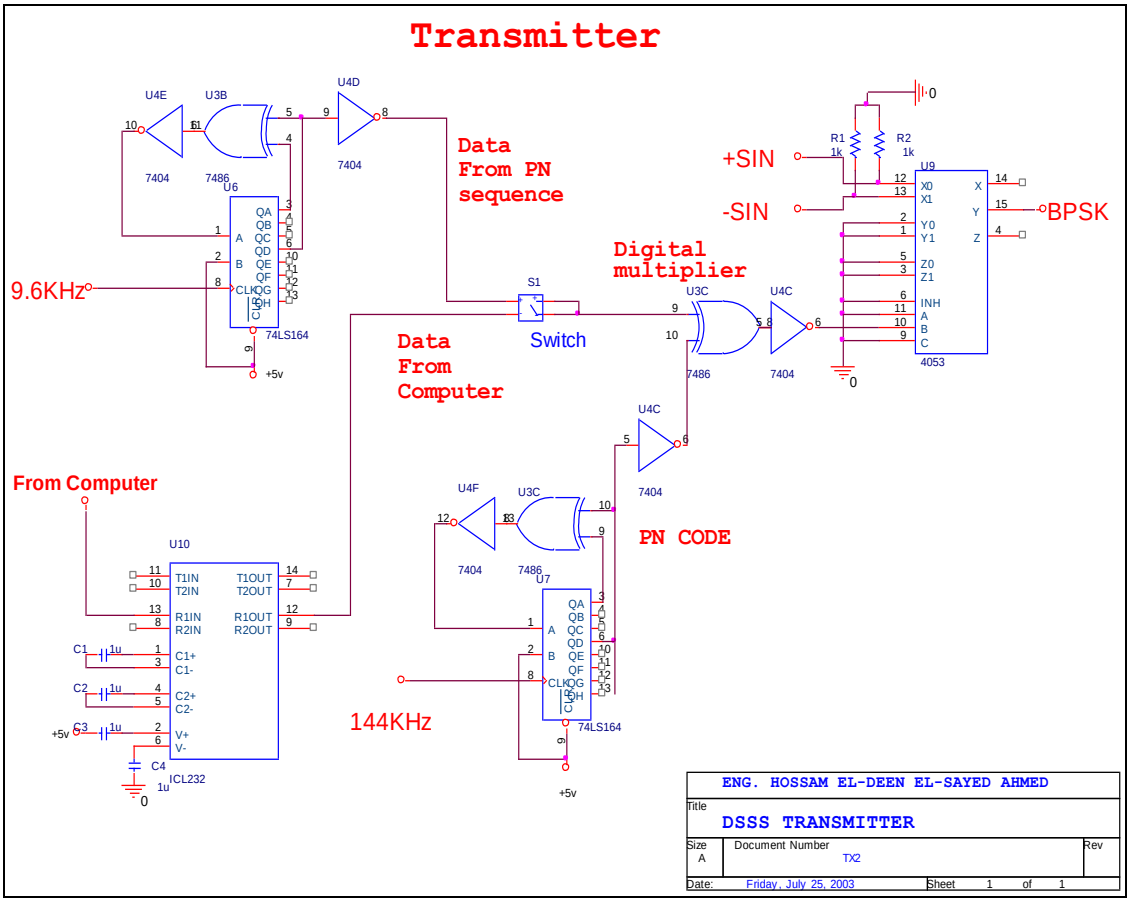


Fig (5) The implemented circuit diagram of Modulating Circuit

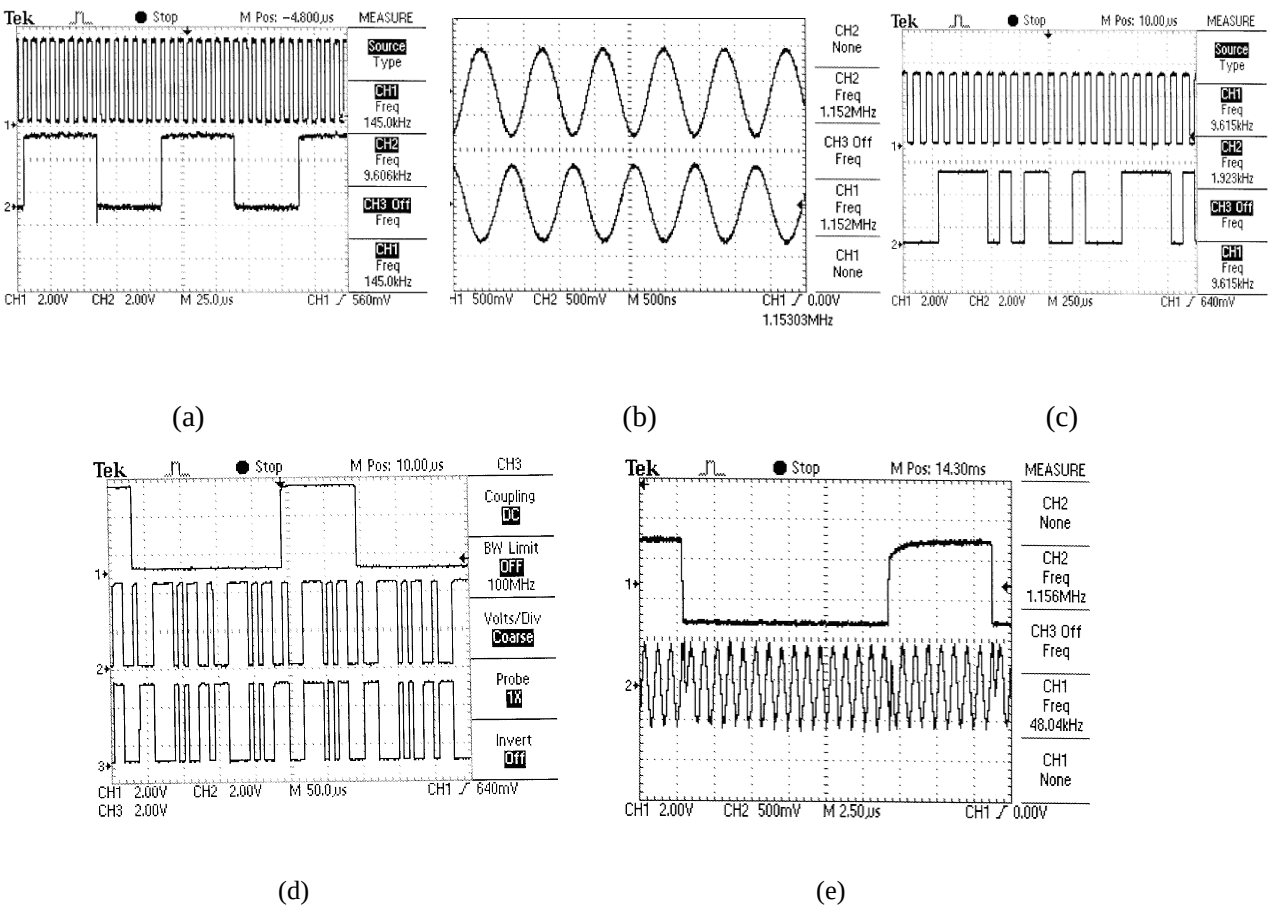


Fig (6) (a) Divide by 15 Stage (b) +SIN & -SIN (c) PN Code Generator (d) Digital multiplier (e) BPSK Modulator

IV. RECEIVER IMPLEMENTATION

The implemented DSSS receiver is divided into two sub circuits. The first circuit is the carrier recovery circuit and the other one is the demodulation circuit.

1- Carrier Recovery Circuit (CRC)

The CRC circuit is used in the receiver to generate a replica of the carrier used in transmitter with the same phase and frequency. This regenerated carrier is used in the demodulation process to recover the data. In the practical implementation a simple circuit is used to generate a signal that is double the frequency of the carrier. This is shown in Fig (7).The received BPSK signal is clipped by a clipping circuit (2 diodes) then applied to an inverter with feedback resistance so that the BPSK signal is converted to a digital form and amplified as shown in Fig (8-a). Then this digital signal is applied to an XOR gate with a delayed version of itself. At XOR inputs each pulse with its delayed version generates 2 pulses at the output of XOR. This circuit is called +VE &-VE edge detector and it has output signal with twice frequency of the input as shown in Fig (8-b).The double frequency signal of 2304 kHz ($2f_c$=2*1152) is then applied to Phase Locked Loop (PLL). The utilized chip 74HCT4046 is a PLL that operates at high frequencies (up to 18 MHz). The VCO output of PLL has 2304 KHz rectangular output as shown in Fig (8-c).The digital output of PLL is then fed to divide by two counter to obtain a regenerated carrier of 1152 KHz and also fed to divide by 16 counter to obtain the clock required to generate the code. The measured

carrier in the transmitter and regenerated carrier in the receiver are shown in Fig (9-a). The original clock of PN code in the transmitter is plotted with recovered clock in the receiver in Fig (9-b).

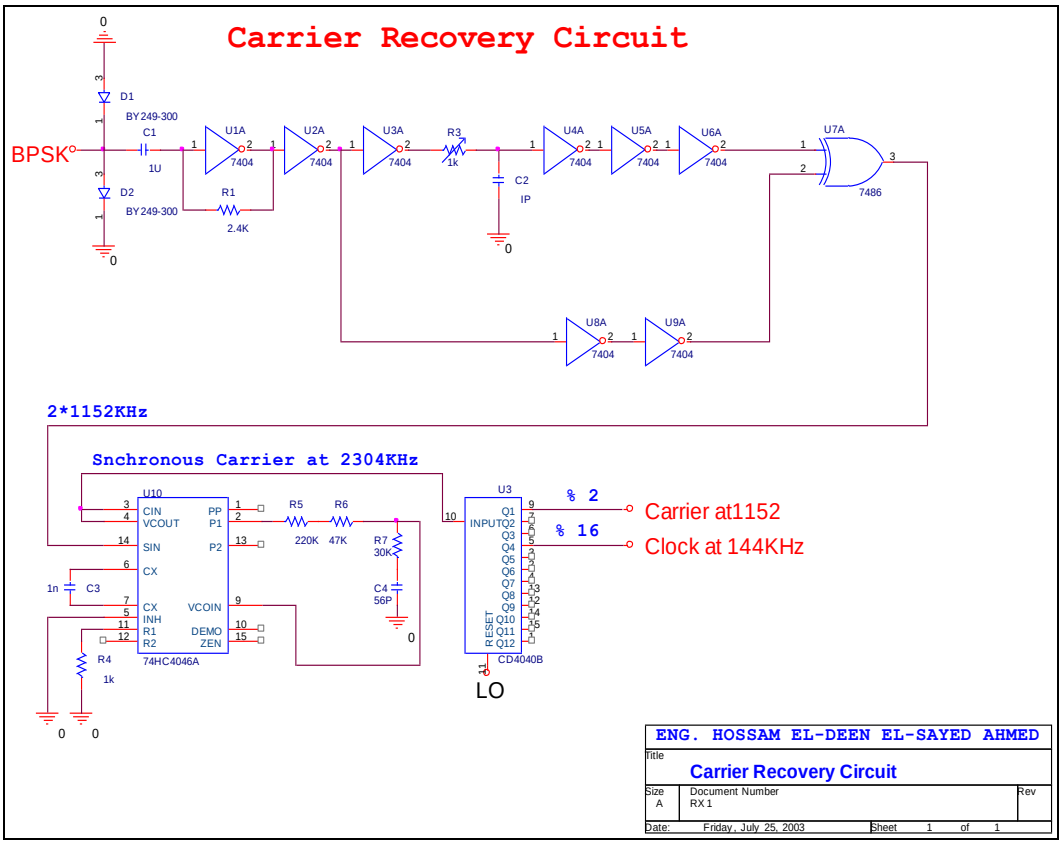
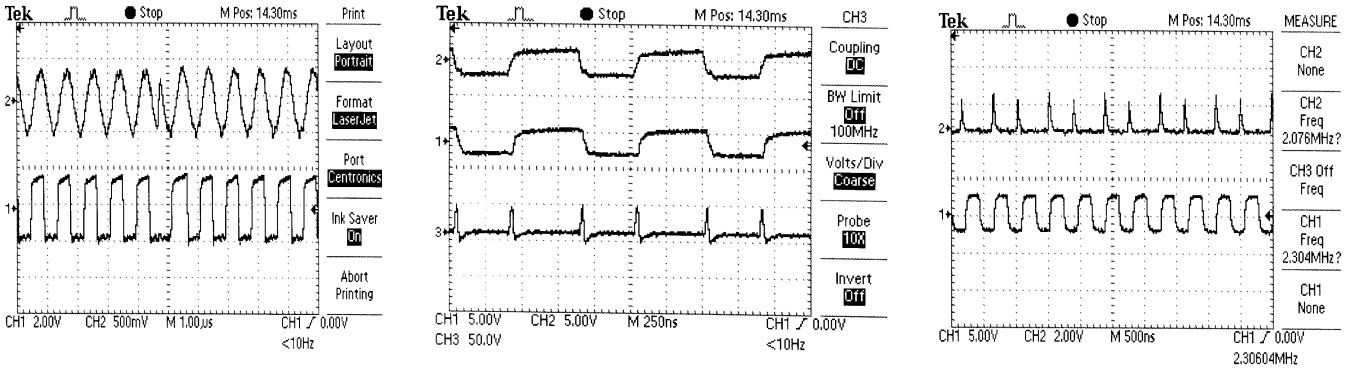
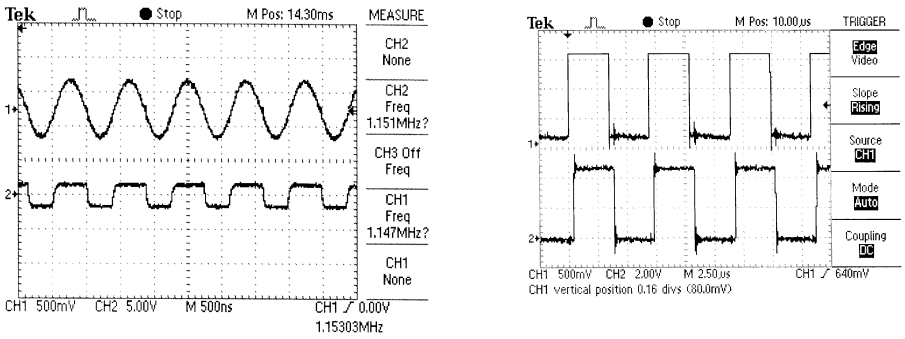


Fig (7) The implemented circuit diagram of Carrier Recovery Circuit



(a) (b) (c)

Fig (8) (a) I/P & O/P of clipping circuit (b) The two inputs & o/p of edge detector (c) i/p &o/p of PLL



(d) (e)

Fig (9) (a) carrier of transmitter & carrier by CRC (b) transmitter clock & recovered clock

2- Demodulating circuit

It has the reverse operation of the modulation circuit of the transmitter. The implemented circuit is shown in Fig (10). The first section of this circuit is the BPSK demodulator which is implemented as that of the transmitter by using analog multiplexer 4053. The received BPSK signal is fed to a buffer and at the same time via an inverter so a +BPSK signal & -BPSK signal are applied at the inputs of the analog multiplexer , the selection between them is made by the recovered carrier from CRC circuit.

At the +ve cycle of the carrier the 4053 passes the +BPSK signal while at the –ve cycle of the carrier the 4053 passes –BPSK signal. This process is equivalent to a multiplication process of BPSK signal and the local generated carrier. The result of this multiplication process is either a +ve voltage which has a time duration equal to the chip time (which is equivalent to logic one chip) or –ve voltage which has a time duration equal to the chip time (which is equivalent to logic zero chip).The measured output of this stage is shown in Fig (11-a). This output is low pass filtered to extract the chip component as shown in Fig (11-b). After the LPF the signal is fed to Schmitt trigger to convert it into digital form. The practical transmitted and received chips are plotted in Fig (11-c).

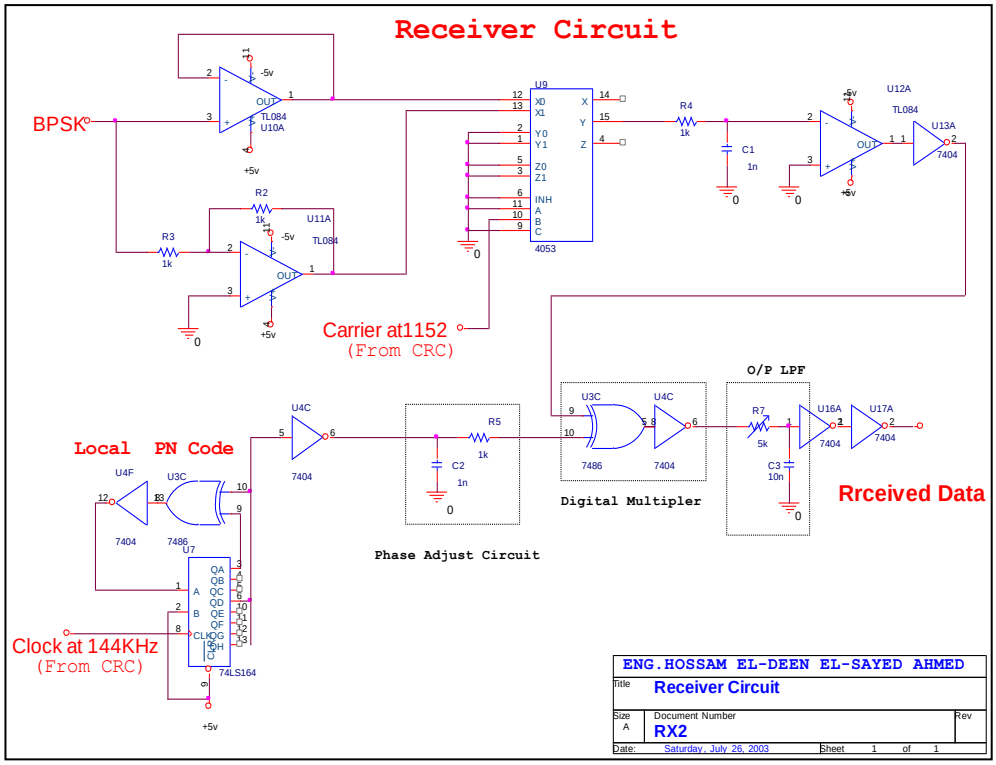
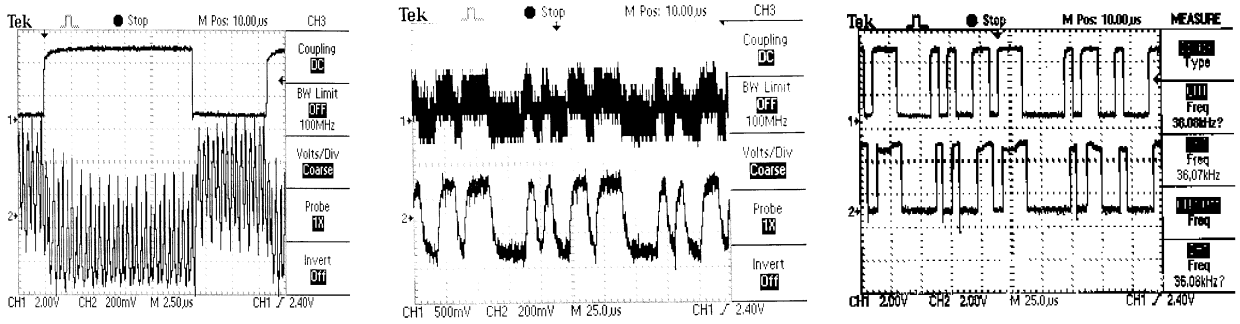


Fig (10) The implemented circuit diagram of Demodulating Circuit



(a) (b) (c)

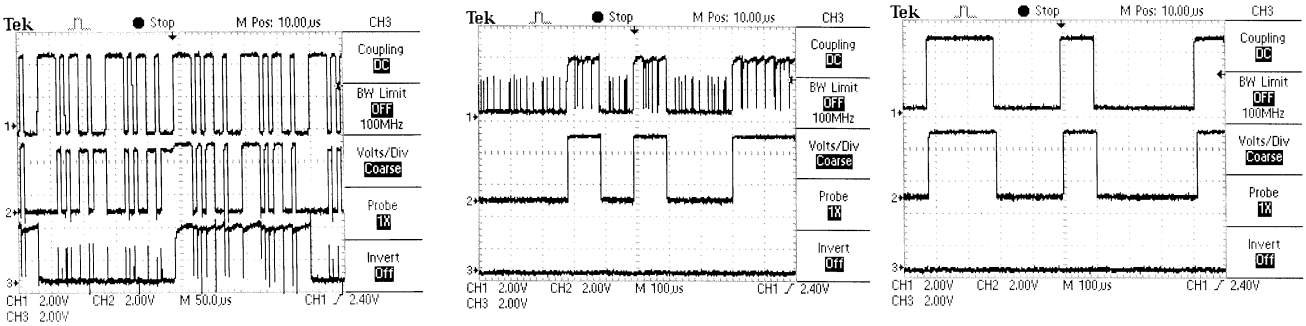
Fig (11) (a) BPSK Demodulator o/p (b) LPF o/p (c) Transmitted chips & Recovered Chips

After the first demodulation process has been done the second demodulation process which is better called the despreading process must take place.

First we use the recovered clock from CRC to generate a replica of the code used in the transmitter. The regenerated code must be the same as the one used in transmitter so the same circuit of transmitter is used again in receiver but with clock from CRC circuit.

The phase of the generated code must also be adjusted with the recovered chips in order that the multiplication process to be correctly done. The adjusting process is done practically to the received chips to make them synchronized with the regenerated code by using a suitable delay circuit. The despreading process is done by applying the synchronized chips and code to the inputs of XNOR to achieve digital multiplication process as shown in Fig (12-a).

As seen from Fig (12-a) the output of the multiplier still has a little phase error leading to the formation of spikes which can be removed by using a LPF as shown in Fig (12-b).Now the despreading process is completed and the data is reproduced successfully, The final received bit stream is plotted with the original transmitted data stream in Fig (12-c). We see that both bit streams coincide with each other proving the correct operation of the implemented transceiver.



(a) (b) (c)

Fig (12) (a) Receved Chips , Code &O/P of Digital Multiplier (b) LPF O/P (c) Transmitted &Received Data

CONCLUSIONS

1- The measured waveforms at different stages of the practically carried out circuits of the system agree well with the simulation results which mean that all the specifications are satisfied.

2- Two models have been proposed concerning the order of the spreading and modulation process. Both have been found to be equivalent because of the system linearity.

However performing the spreading first leads to spikes in the demodulated symbol but it is easier to implement practically.

References

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